



**PATENT**  
**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF : TECHNOLOGIES LTRIM INC.  
FOR : METHOD FOR MODIFYING THE  
IMPEDANCE OF SEMICONDUCTOR  
DEVICES USING A FOCUSED HEATING  
SOURCE  
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**TRANSMITTAL LETTER OF 35 U.S.C. § 119**  
**AND FILING OF FOREIGN PRIORITY DOCUMENT**

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Madam, Sir;

The applicant hereby claims priority under 35 U.S.C. § 119 for the above-identified U.S. patent application. This claim of priority is based upon Canadian Application for Patent Serial No. 2,398,166 filed on August 14, 2002.

The applicant joins herewith a certified copy of the Canadian priority.



Respectfully submitted,

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Specification and Drawings, as originally filed, with Application for Patent Serial No:  
**2,398,166**, on August 14, 2002, by **TECHNOLOGIES LTRIM INC.**, for "Method for  
Modifying the Impedance of Semiconductor Devices Using a Focused Heating Source".

*Mary Lavallee*  
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## ABSTRACT OF THE DISCLOSURE

A method is provided for tuning (i.e. modifying, changing) the impedance of semiconductor components or devices using a focused heating source. The method may be exploited for finely tuning the impedance of semiconductor components or devices, by modifying the dopant profile of a region of low dopant concentration (i.e. increasing the dopant concentration) by diffusion of dopants from adjacent regions of higher dopant concentration through the melting action of a focused heating source, for example a laser. The present invention is in particular directed to the use of lasers in relation to circuits for the creation of conductive links and pathways where none existed before. The present invention more particularly relates to a means wherein impedance modification (i.e. trimming or tuning) may advantageously be carried out as a function of the location of one or more conductive bridge(s) along the length of a gap region.

**METHOD FOR MODIFYING THE IMPEDANCE OF  
SEMICONDUCTOR DEVICES USING A FOCUSED HEATING SOURCE**

5       The present invention relates to the field of semiconductor components or devices,  
and is directed to a method and apparatus for tuning (i.e. modifying, changing) the  
impedance of semiconductor components or devices using a focused heating source.  
The method may be exploited for finely tuning the impedance of semiconductor  
10       components or devices, by modifying the dopant profile of a region of low dopant  
concentration (i.e. increasing the dopant concentration) by diffusion of dopants from  
adjacent regions of higher dopant concentration through the melting action of a  
focused heating source, for example a laser. The present invention is in particular  
directed to the use of lasers in relation to circuits for the creation of conductive links  
and pathways where none existed before. The present invention more particularly  
15       relates to a means wherein impedance modification (i.e. trimming or tuning) may  
advantageously be carried out as a function of the location of one or more conductive  
bridge(s) along the length of a gap region.

20       Modifying the impedance of a (integrated) semiconductor device or component  
through the use of lasers is known in the art. Such methods, sometimes known as  
laser trimming of (integrated) semiconductor devices is most often performed on a  
semiconductor device or component having a resistive thin film structure,  
manufactured with materials such as silicon chromide, cesium silicides, tantalum  
nitride or nichrome. The trimming of the (integrated) semiconductor device or  
25       component, in order to achieve a required or desired impedance value may be  
obtained by laser ablation, (i.e. by evaporation, or burning off), of a part of the  
resistive thin film. In other word, the laser is used to evaporate a portion of a resistive  
thin film structure, which due to the change in the amount of resistive thin film that  
remains, causes a change in the impedance value of the (integrated) semiconductor  
30       d vice.

It is also known to it ratively selectively tuning the impedance of (integrat d)  
semiconductor devices or components, by modifying the dopant profile of a region;

see for example US Patent no. 6,329,272 the entire contents of which is incorporated herein by reference.

5 It would be advantageous to have relatively simple means for lowering the resistance (i.e. impedance) of integrated resistors, i.e. to be able to use lasers or other focussed heat sources to modify the impedance, i.e. decrease the impedance of an integrated semiconductor device. It would also be advantageous to have an  
10 alternative method for iteratively, selectively tuning the impedance of integrated semiconductor devices through the use of a focussed heating source, such as a focussed laser beam. It would also in particular be advantageous to be able to lower the impedance of an integrated semiconductor device by creating one or more secondary conductive paths, (i.e. electrically conductive path(s)) rather than (solely) by attempting to accurately control the diffusion of dopant from one region to another.

15 It would be advantageous to have a semiconductor device or component wherein in accordance with the present invention the base (or main) conductive path of the device has an initial (i.e. non-infinite) impedance (e.g. non-infinite resistance) and has a configuration whereby the main conductive path is capable of being trimmed or  
20 tuned by decreasing such impedance.

Therefore, the present invention, in accordance with a general aspect provides for a method for modifying the impedance of a semiconductor component, said semiconductor component comprising

25 a first conductive region defining a base (i.e. initial) conductive path, said first conductive region comprising a first link portion and a second link portion, said first region having a heat modifiable dopant profile

and

30 a second region contiguous with the first region, said second region having a dopant profile rendering said second region non-conductive relative to said first region,

said first and second link portions being disposed in juxtaposition such that said first and second link portions are separated by a gap region defined by said second region, said second region having a heat modifiable dopant profile, at least with respect to said gap region,

5           said method comprising applying a bridging cycle to at least one preselected area, each said preselected area comprising at least a portion of each of said first link portion, said second link portion and said gap region, so as to form a discrete conductive bridge across said gap region and connecting said first link portion and said second link portion,

10           said bridging cycle comprising a heating/cooling treatment comprising  
                     directing a focussed heating source to melt said preselected area and to thereby alter the dopant profile of the pre-selected area  
                     and

15           allowing said melted pre-selected area to solidify with an altered dopant profile so as to form thereby said discrete conductive bridge.

The present invention in accordance with another aspect provides a method for modifying the impedance of a semiconductor device or component, said semiconductor device or component comprising

20           a first conductive region comprising a conductive crimp element, (i.e. at least a part of the first conductive region being disposed in the form of a conductive crimp or fold element), said first region having a heat modifiable dopant profile, said conductive crimp element defining an  
 25           base (i.e. initial) conductive path,

and

                    a second region contiguous with the first region, said second region having a dopant profile rendering said second region non-conductive relative to said first region,

30           said crimp element comprising a first link portion and a second link portion, said first and second link portions being disposed in juxtaposition such that said first and second link portions are separated by a gap region defined by said

second region, said second region having a heat modifiable dopant profile at least with respect to said gap region,

said method comprising applying a bridging cycle to at least one preselected area, each said preselected area comprising at least a portion of each of said first link portion, said second link portion and said gap region, so as to form a discrete conductive bridge across said gap region and connecting said first link portion and said second link portion,

said bridging cycle comprising a heating/cooling treatment comprising

directing a focussed heating source to melt said preselected area and to thereby alter the dopant profile of the pre-selected area

and

allowing said melted pre-selected area to solidify with an altered dopant profile so as to form thereby said discrete conductive bridge.

The present invention in accordance with a further aspect provides for a method for modifying the impedance of a semiconductor component, said semiconductor component comprising

a first conductive region comprising a first conductive link portion and a second link portion, said first region having a heat modifiable dopant profile, said first conductive link portion defining a base (i.e. initial) conductive path

and

a second region contiguous with the first region, said second region having a dopant profile rendering said second region non-conductive relative to said first region,

said first and second link portions being disposed in juxtaposition such that said first and second link portions are separated by a gap region defined by said second region, said second region having a heat modifiable dopant profile, at least with respect to said gap region,

said method comprising applying a bridging cycle to at least one preselected area, each said preselected area comprising at least a portion of each of said first



link portion, said second link portion and said gap region, so as to form a discrete conductive bridge across said gap region and connecting said first link portion and said second link portion,

5        said bridging cycle comprising a heating/cooling treatment comprising  
              directing a focussed heating source to melt said preselected area and  
              to thereby alter the dopant profile of the pre-selected area  
              and  
              allowing said melted pre-selected area to solidify with an altered dopant  
 10        profile so as to form thereby said discrete conductive bridge.

It is to be understood herein that the word "impedance" relates to both resistance and capacitance, and that modifying the impedance of an integrated semiconductor device is understood to comprise modifying the resistance and/or the capacitance of  
 15        a semiconductor device or component, as the case may be.

In accordance with the present invention it is to be understood herein that the reference to a "base conductive path" (i.e. initial conductive path) of a device or component is a reference a conductive path having an initial (i.e. non-infinite)  
 20        impedance (e.g. non-infinite resistance) prior to tuning or trimming as discussed herein.

In accordance with the present invention, a method as described herein may further include the steps of

25        a) determining the impedance of said semiconductor device component subsequent to a bridging cycle and  
              b) comparing the impedance obtained from step a) with a predetermined impedance

and

30        c) if necessary, repeating, at one or more additional pre-selected areas, said bridging cycle, until said predetermined impedance is achieved, each bridging cycle being applied to a different pre-selected area to form a respective discrete conductive bridge.

In accordance with the present invention if more than one conductive bridge is needed or deemed necessary, any such additional conductive bridge(s) may be disposed on either side of the initial conductive bridge.

5 As may be appreciated, in accordance with the present invention, impedance modification (i.e. trimming or tuning) may advantageously be carried out as a function of the location of a conductive bridge along the continuous length of the gap region.

10 In accordance with the present invention, a crimp element may take on any suitable, desired, appropriate or necessary configuration keeping in mind that the first and second link portions thereof are to be disposed in juxtaposition such that the first and second link portions are separated by a gap region defined by the second region and that the crimp or fold element is to define a (main) conductive path. The gap region may for example have a constant width or a width which increases or decreases in  
15 size. Thus for example, a conductive crimp element may have a U-like shape wherein the lateral arms or legs of the U-shaped crimp element are interconnected by a spacer portion. The first and second link portions may each have a respective first contact or connection end for electrically connecting the crimp element other elements of a semiconductor device. The spacer portion is connected to each of the  
20 first and second link portions at a position away from the respective first ends of the first and second link portions.

Alternatively the crimp or fold element may have a H-like shape, a saw-tooth like shape etc..

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As a further alternative the first conductive region may define two or more ( e.g. adjacent or spaced) crimp or fold elements . The first conductive region may for example define two or more adjacent crimp or fold elements such that the first  
30 conductive region may have, a V-like shape, a W-like shape, a zig-zag-like shape or the like.

As may be understood a discrete conductive bridge as formed herein defines a secondary conductive path which electrically connects the first link portion and the second link portion across the gap region.

5 In accordance with the present invention the semi-conductor component or device, before trimming or tuning as described herein, is already an electrical conductor having an initial (non-infinite) impedance which may already be near the sought after value, i.e. the initial value is higher than the desired end value. This means that the device or semiconductor component may be tested even before being subjected to  
10 the laser tuning process.

More particularly, in accordance with the present invention the impedance of a device may be altered, inter alia, as a function of the position and number of discrete conductive bridges in relation to a conductive crimp element.

15

In other words, if a semiconductor device or component

a) is provided with one or more a conductive crimp or fold elements, and

b) each crimp or fold element has an appropriate configuration

20

i) so as to define an initial or base conductive path (i.e. of non-infinite impedance, )

and

ii) so as to have at least one gap region (i.e. a gap spannable by a heat produced discrete conductive bridge) spacing apart opposed portions of the initial or base conductive path,

25

the physical location and the number of discrete conductive bridges spanning a given gap region, may advantageously be used as parameters or adjustment or tuning factors for adjusting the impedance (e.g. resistance) of the base conductive path of the device or component.

30

It is to be understood herein that the expression "heat modifiable dopant profile" characterizes a region or area (as the case may be) as being one which may, on the application of a suitable heat source, be melted such that dopant may migrate or

diffuse there through so as to alter the dopant profile thereof which may be maintained on solidification of the melted area.

Another advantage of the present invention relates to the temperature coefficient for the device or semi-conductor component; the variation of the temperature coefficient of the laser link(s) (i.e. laser produced bridges) may only hardly or weakly affect the overall temperature coefficient of the device since the laser link(s) may be so configured as to contribute in only a small part to the total overall resistance (i.e. impedance) of the device.

A further advantage of the present invention relates to the long term stability of the device or semi-conductor component; the variation of the long term stability of the laser link(s) may only hardly or weakly affect the overall long term stability of the device since the laser link(s) may be so configured as to contribute in only a small part to the total overall long term stability of the device.

In accordance with the present invention, a laser produced link (i.e. bridge) between opposed portions of the main conductive path may account for only a part of the total desired resistance (i.e. impedance) of the device. Therefore to obtain a tolerance of 0.1% with respect to the total resistance (i.e. impedance) of the device, the required tolerance with respect to the resistance (i.e. impedance) of the laser induced links may perhaps each only need be on the order of 1.0%. The ability to relax the level of precision for the production of the laser links means less control needs to be applied to the tuning process and can lead to a faster laser tuning process.

Depending on the dimension and/or geometry of a semiconductor device or component it may be possible to achieve resistance tolerance as low as 0.001%.

In accordance with an embodiment of the present invention, there is provided for a method of tuning (i.e. modifying or decreasing) the impedance of an (integrated) semiconductor device or component through the exploitation of one or more bridging cycles each of which induces the diffusion of dopants from side or lateral areas having a high dopant concentration (i.e. a high  $r$  concentration) to an intermediate (i.e. gap) area of lower dopant concentration.

In accordance with the present invention a conductive link may be obtained by application of a single laser pulse; alternatively a conductive link may be obtained by the application of a series of pulses such as for example as described in above mentioned US Patent no. 6,329,272.

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In accordance with the present invention a conductive bridge may, if so desired or appropriate be formed by a controlled diffusion, i.e. it may be formed by a careful, calculated and measured application of focused energy being applied to the integrated semiconductor device, which may result in a controlled and/or determinable quantity of dopants being diffused from one area to an adjacent area having a lower dopant concentration.

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Alternatively, in accordance with the present invention, a conductive bridge may, advantageously, be formed from the application of an indiscriminate pulse from a high powered laser (i.e. a blast of energy); the pulse spanning across the gap region over a part of each of the link portions and being applied so as to provide (under pre-given conditions) a degree of diffusion which may vary from the minimum amount of diffusion (necessary to provide a conductive bridge) to a maximum amount of diffusion which likewise results in a desired conductive bridge.

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In accordance with the present invention, semiconductor devices may be tuned, which expression (tuned or tuning) is understood to mean that the impedance of the integrated semiconductor device may be modified, adjusted, changed, (i.e. decreased). It is further understood that fine tuning of an integrated semiconductor device is understood to mean that the impedance, once it has been grossly obtained (i.e. by the initial manufacturing process of laying down appropriate layers, substrates etc.), may be finely tuned (i.e. finely adjusted, or with high precision). Fine tuning may involve a single step or a distinct series of steps.

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In accordance with an embodiment of the present invention, the tuning of an integrated semiconductor device may be accomplished iteratively, i.e. through the use of an iteration technique or method. Thus, iteratively or iteration technique is to be understood to mean a process, action or procedure in which repetition of a

sequence of operations yields results which are successively closer to a desired result. Therefore, the objectives of a particular embodiment of the present invention may be accomplished through the use of an iteration technique, by which the successive application of heat (i.e. one or more pulses) from a focussed heating source to different areas, may progressively yield an impedance profile which is progressively closer to the required or desired profile across a given integrated semiconductor device.

For example, a first laser application (i.e. first bridge cycle) to a first location may result in 80 % of the required impedance change, a second laser application (i.e. second bridge cycle) to a second location may result in 91% of the required impedance change, a third laser application (i.e. third bridge cycle) to a third location may result in 98% of the required impedance change, and a fourth laser application (i.e. fourth bridge cycle) to a fourth location may result in 100% of the required impedance change. It is understood however that a greater or lesser number of laser applications may be required to achieve the required or desired impedance change, and it is further understood that the required impedance change may be achieved with as little as one or two laser applications.

In accordance with a general embodiment of the present invention, an integrated semiconductor device may comprise a number of components. Included among these may be areas which may be doped with dopants, such as for example, n type or p type dopants. The dopant concentration of various areas of a device may vary according to their use and application, and there may be, for example, areas of a given dopant concentration, and adjacent thereto there may be areas of higher or lower dopant concentration. In accordance with an embodiment, there may therefore be a pair of first areas of a predetermined or selected dopant concentration, and an adjacent intermediate second area of a (relative) lower dopant concentration. As may be understood, the difference in the dopant concentration between areas may be sufficient such that the physical and electrical properties of each of the areas may be different, i.e. for example, one may conduct electrical current, while the other may not, or their relative capability to conduct electrical current may be different. The present invention therefore addresses a method for modifying the relative current

carrying capacities of adjacent areas of an integrated semiconductor device by modifying the relative dopant concentration difference of said areas.

By way of example, in accordance with the present invention, in order to modify the relative dopant concentration difference between first doped areas and an intermediate second doped area having a lower dopant concentration, the following iterative steps may be effected. Namely, a focussed heating source may be targeted at a selected area, which selected area may comprise therein a portion of the first doped areas, and a portion, or the intermediate second doped area, i.e. the selected area may straddle the boundary between the first and the second doped areas. As may be understood, the selected area may be generally round, and may or may not evenly straddle the boundaries between the first and the second doped region.

The target area or location for a first conductive bridge may be determined by first testing the actual impedance (e.g. resistance) of the base or main conductive path; determining the resistance/unit length for the base path; determining the amount by which the resistance must be lowered (i.e.  $\Delta R$  resistance) to reach a desired predetermined overall resistance; determining the path length equivalent to the  $\Delta R$  resistance; and then calculating the position of a desired conductive bridge across the gap region which will provide an at least initial desired overall lowering of the resistance. As may be appreciated such calculations may be based on known equations for the calculation for series, parallel, series-parallel, etc. circuits. This may of course be done by an appropriately configured computer means.

Once the selected location or area has been targeted, there may be applied to the selected area a (heating) pulse from a focused heating source, which heating pulse causes the selected area to melt, i.e. to change from the solid stated to the liquid state. As may be understood, portions of the first doped areas and portions of the second doped area which are outside of the selected area will not be caused to be melted by the application of the heating pulse.

The period during which the selected area may be melted may be long or short, (e.g., of the order of 10 femtosecond to 10 microseconds long). In any event the period of

time during which the selected area may be melted is of course to be sufficient to allow the diffusion (i.e. migration) of dopants from the first areas to the second area of lower dopant concentration. The diffusion of dopants from an area of higher dopant concentration to an area of lower dopant concentration occurs in accordance with well known principles. The (controlled) diffusion may therefore take place very rapidly, such that even during a short time during which the selected area may be melted, sufficient dopants may diffuse which may cause an appreciable change in the dopant concentration of the area of lower dopant concentration.

As mentioned, the melted area may only remain in a liquid state for a short period of time, i.e. for a period of time substantially the same as the length of application of the heating pulse. Once the selected melted area has solidified, the dopant profile of the selected area may therefore have been modified, and may therefore be of a concentration which is intermediate the dopant concentration of the first areas and the second area of lower dopant concentration.

Once the preceding step has been accomplished, further steps in an iterative process may be undertaken. For example, the next step may comprise the determination, i.e. the testing of the new impedance of the integrated semiconductor device achieved as a result of the application of the first heating pulse. This testing may be conducted in accordance with any known or desired method, and the results may be compared with the required or desired end result.

Depending on the impedance value of the integrated semiconductor device achieved as a result of the prior iterative steps and depending on the final impedance which is required or desired, it may be necessary to perform a further iterative step of the method. For example, if the impedance has not been sufficiently decreased, a further application of a focused heating source may be made to a different pre-selected area (i.e. different location) in order to further decrease the impedance. Namely, the application of a further (i.e. second) focused heating source may further melt (all, or part of) the other pre-selected area of the integrated semiconductor device, thus forming an additional conductive bridge, as described above.



Once the additional melted area has solidified, a further step in the iterative process may involve the re-testing of the resulting impedance and the comparison of this resulting impedance with the required desired result. If the resulting impedance is still not what is required or desired, a further iterative step may be performed similar to the process as described above.

As may be understood, in accordance with an example embodiment of the present invention, the iterative process involves in its most general form the application of a heating pulse which may cause a modification in the relative dopant concentration of adjacent and abutting areas of an integrated semiconductor device, the testing of the impedance resulting from the application of said heating pulse, and if required or desired, the repetition of the bridge cycle. As may be further understood, subsequent to the determination of the resulting impedance following the application of a heating pulse, some or all of the characteristics of the subsequent heating pulse or pulses may be modified, i.e. adjusted. The characteristics of the heating pulses which may be modified are varied, and may depend on how much of a further modification of the impedance the next application of the heating pulse is required to achieve. Thus, for example, if after the application of one heating pulse, it is determined that the impedance has reached a substantial percentage of the required result, the characteristics of the next focused heating pulse may be modified, as an example, the power of the focussed heating source may be decreased. As a further example, the length of the application of the heating pulse may be decreased, all in order to bring the impedance as close as possible to a required result. Further, the angle of application of the heating source may be varied, i.e. varied from a 90° angle application. In addition, a different heating source may also be employed. Subsequent to the application of a modified heating pulse, if the integrated semiconductor device is further tested and it is determined that, for example, substantially all of the required or desired impedance change has been achieved, the characteristics of the heating pulse may be further modified, i.e. the power of the heating pulse may again be further reduced, the length of application of the heating pulse may also be further reduced, etc... It is however possible that the characteristics of any of the subsequent heating pulses may be increased for a subsequent application, i.e. some or all of the power of the heating pulse, the length of

application, etc... may be increased. In other words, not all of the applied heating pulses may be identical, however it is foreseen that as the impedance is iteratively brought closer to the desired end-value, the characteristics of the focused heating source may be decreased, or lowered.

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More particularly, in accordance with of the present invention, there may be provided for an integrated semiconductor device which may be configured and disposed such that it comprises, two conductively interconnected areas or regions of relatively high dopant concentration which are spaced apart by a gap area or region of a relatively lower (or no) dopant concentration. Thus the area of lower (or no) dopant concentration may act as an insulator, between the two areas of higher dopant concentration. The dopant type and/or concentration thereof of the area of lower dopant concentration may be of a type and/or of a low enough concentration such that no or at least essentially no electrical current may flow there through.

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It is understood that for some electrical current to pass through a bridge area of lower dopant concentration disposed between two areas of higher dopant concentration, it is necessary to arrange that the type of dopant in the three areas be identical, i.e. either all of n type, or all of p type. In accordance with this embodiment, the method of the present invention may be used to modify the dopant concentration of a part of the gap region thereof, therefore decreasing the preexisting impedance of any part of an integrated semiconductor device. In other words the use of the method of the present embodiment may allow for the impedance of an integrated semiconductor device to be modified such that some electrical current (i.e. as opposed to no electrical current) may be able to flow across a conductive bridge spanning a gap region.

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The type of dopant (or dopants) used in the lightly (i.e. lower) doped region may, however, not be the same as the type of dopant use in the heavily (i.e. higher) doped regions. For example, if the heavily doped region uses a p type dopant, the lightly doped region can be either p type or n, and vice versa. It is understood that in this case, the amount of dopant to be diffused from the area (or areas) of higher dopant concentration into the area of lower dopant concentration may need to be high

enough to counter the presence of the different type of dopant present in the lightly doped area, such that current may flow through said lightly doped area.

5 The level of concentration of the dopants in the areas of high and low concentration may vary significantly. For example, the dopant concentration may vary between  $10^{12}$  to  $10^{20}$  atoms per  $\text{cm}^3$ . The range of dopant concentration for a lightly doped area may, for example, be between  $10^{12}$  to  $10^{16}$  atoms per  $\text{cm}^3$  while the dopant concentration for an area of high dopant concentration may, for example, be between  $10^{16}$  to  $10^{20}$  atoms per  $\text{cm}^3$ . In any event, the dopant concentration(s) may be those  
10 (normally) encountered in industry, i.e. they may be higher or lower than mentioned hereinabove..

15 It is understood that the terms lightly doped region and heavily doped region are not meant to exclude a first doped region which dopant concentration is only slightly higher than a second doped region (depending on dopant type). The dopants which may be used in accordance with the present invention may be selected from the group comprising boron, phosphorus, aluminum, antimony, arsenic, gallium, indium, lithium, thallium and bismuth. The dopants may be doped in a substrate comprising a material selected from the group comprising silicon, gallium arsenide, silicon-germanium, compounds selected from columns III-V and II-VI of the periodic table,  
20 and compounds having a IV-IV alloy.

25 The focussed heating source which may be used in accordance with the present invention may be selected from a group comprising a laser and an electron beam. Further, the energy of the heating pulses of said focussed heating source may be low enough to avoid damaging the integrated semiconductor device.

30 Example embodiments of the present invention are illustrated in the drawings herein;

FIG. 1 illustrates schematically an example of a tunable semiconductor component or device in accordance with the present invention, wherein the first conductive region is disposed in the form of a conductive crimp element having a U-like shape configuration or pattern;

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FIG. 2 illustrates schematically another example of a tunable semiconductor component or device in accordance with the present invention, wherein the first conductive region is disposed in the form of a conductive crimp element having a H-like shape configuration or pattern;

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FIG. 3 illustrates schematically another example of a tunable semiconductor component or device in accordance with the present invention, wherein the first conductive region is disposed in the form of a conductive crimp element having a V-like shape configuration or pattern;

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FIG. 4 illustrates schematically another example of a tunable semiconductor component or device in accordance with the present invention, wherein the first conductive region is disposed in the form of a conductive crimp element having a W-like shape configuration or pattern;

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FIG. 5 illustrates schematically another example of a tunable semiconductor device in accordance with the present invention, wherein the first conductive region is disposed in the form of a plurality (i.e. 3) conductive crimp elements each having a U-like shape configuration or pattern;

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FIG. 6 illustrates an electric schematic of a tuned semiconductor component or device having the aspect of the device of Fig. 5 but with only two conductive bridges;

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FIG. 7 illustrates a cross-sectional view of through a bridge of the tunable integrated semiconductor device as shown in Figure 5;

FIG. 8 illustrates a schematic view of the laser system used for the tuning process;

FIG. 9 illustrates a more complete view of the schematic view of the laser system shown in Figure 8;

FIG. 10 illustrates an example electric schematic of a series resistor ladder which may be used in an analogue to digital converter;

FIG. 11 illustrates how a plurality of the integrated semiconductor device as shown in Figure 5 may be disposed so as to define the series resistor ladder of figure 10;

FIG. 12 illustrates an example electric schematic of an R-2R resistor ladder which may be used in a digital to analogue converter;

FIG. 13 illustrates how a plurality of the integrated semiconductor device as shown in Figure 5 may be disposed so as to define the R-2R resistor ladder of figure 12;

FIG. 14 schematically illustrates an example of another tunable integrated semiconductor device of the present invention wherein one of the link portions of the crimp or fold element is not (initially) in the main conductive path; and

FIG. 15 schematically illustrates an example combination of an integrated semiconductor device as shown in Figure 5 with an integrated semiconductor device as shown in Figure 14 to provide a device of higher precision than would be obtainable by the device of FIG. 5 alone.

Figures 1 to 5 illustrate example embodiments of a tunable semiconductor component or device in accordance with the present invention. For each of Figures 1 to 5 the tunable semiconductor component or device is generally designated by the reference numeral 1. The device 1 in each case may comprise various layers or regions, for example, a non-conductive substrate 2, and a conductive layer or region 2a which is contiguous with the underlying substrate 2.

The regions 2 and 2a may each comprise semiconductor materials such as silicon, germanium, gallium arsenide, silicon-germanium or other suitable semiconductor materials selected from a group comprising elements from columns III - V, or columns II - VI of the periodic table, or compounds having a IV-IV alloy.

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The region 2a is a heavily doped region, i.e. an electrically conductive region having a heat modifiable dopant profile. As mentioned above, the expression "heat modifiable dopant profile" characterizes a region or area (as the case may be) as being one which may, on the application of a suitable heat source, be melted such that dopant may migrate or diffuse there through so as to alter the dopant profile thereof which may be maintained on solidification of the melted area.

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The region 2a as illustrated in Figures 1 to 5 has a first link portion 3 and juxtaposed therewith a second link portion 4. Referring in particular to Figures 1 and 5, the devices illustrated also have a spacing link portion 4a which links the first and second portions together. The first and second link portions are spaced apart by gap region 5 which is defined by the general region 2. The gap region 5 may, as shall be discussed in more detail with respect to Fig. 5, be spanned by one or more conductive bridges. The device also has contact or connector members 8 and 9 for electrically connecting the region 2a to other devices, current is at least initially able to pass through the entire region 2a between these contact members.

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As may be understood, a heavily doped region may be heavily doped with either n or p type dopants in sufficient concentrations, and of a required or desired profile such that the heavily doped region is electrically conductive. For example, the dopants may be phosphorous, and may be of a concentration of the order of between  $10^{16}$  to  $10^{20}$  atoms per  $\text{cm}^3$ . The thickness of the heavily doped regions may for example be of 0.25 micrometers, but may be greater or lesser in accordance with the requirements of a given manufacturing process. Further, the configuration and disposition of such a heavily doped region may also be in accordance with the requirements of a given manufacturing process.

30

The region 2 as mentioned above comprises the gap region 5 which is disposed intermediate the first and second link portions 3 and 4 of the region 2a. The gap region 5 may have width dimension which, in light of the initial fabrication process, may for example, vary from the minimum size possible up to about 20 microns or more; the gap width may for example vary in accordance with the type of heat pulse treatment to be used; e.g. if a single pulse is to be used then as small a width as possible may be in order; if a series of heat pulses is to be used then a large width may be contemplated.

The region 2 has a dopant profile such that it is electrically non-conductive relative to the region 2a. Thus, the region 2 may comprise no dopant or be a lightly doped region. In any event, the region 2a as in the case of the region 2, at least in the gap region has a heat modifiable dopant profile. The gap region 5 may have a dopant profile which is the same as that of the rest of region 2; alternatively, the gap region 5 may have a dopant profile which is different from that of the rest of the region 2 provided that the dopant profile of the gap region is nevertheless such that the gap region is electrically non-conductive relative to the region 2a and in particular relative to the first and second link portions 3 and 4 thereof.

If a region is lightly doped it may be doped with the same dopant as the heavily doped region, or alternatively, may comprise a different dopant than that present in the adjacent heavily doped region. A lightly doped gap region 5 may be disposed to be adjacent to and abutting heavily doped first and second link portions 3 and 4. The type and concentration level of dopants in a lightly doped gap region 5 may be such that, prior to the application of the method steps in accordance with an embodiment of the present invention, no electrical current may flow across the gap region 5 between heavily doped portions 3 and 4, i.e. wherein the resistance of lightly doped region 5 is high enough to prevent (most if not all) electrical current to flow between heavily doped portions 3 and 4. As may be understood, if the type of dopant of the lightly doped region is different from the type of dopant of the heavily doped region, the device will be equivalent to two diodes in opposite polarity which will not allow any electrical current to pass there through.

Although not shown in Figures 1 to 5 the semiconductor component or device may comprise an overlying passivation layer, such as silicon nitride  $\text{Si}_3\text{N}_4$ . Further, the device may also comprise an oxide layer underlying the passivation layer, such as silicon dioxide  $\text{SiO}_2$ .

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Figure 5 shows a component or device with three crimp elements wherein the link portions of one crimp element may serve as a common link elements for an adjacent or neighboring link element; the crimp elements thus have a serpentine like aspect.

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For illustration purposes only the link portions of the central crimp element are designated with the reference numerals 3 and 4. The three crimp elements may have a width of about 9 microns and a height of about 11 microns. The central crimp element is shown with two discrete solidified conductive bridges or links 10 and 10a spanning across gap region 5, each of bridges 10 and 10a respectively conductively connecting the first link portion 3 and the second link portion 4, i.e. bridges 10 and 10a respectively forming secondary conductive links. The bridge or links 10 and 10a may, for example, independently vary from low resistance links such as a few ohms (e.g. 500 ohms) to links with a resistance for example of up to 100K ohms.

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Although the structure as shown for Figure 5 is, by way of example, shown as having two conductive bridges 10 and 10a, the structure may as desired or necessary have one or more additional conductive bridges disposed up or down the gap region 5. Thus any such additional conductive bridge(s) may be disposed on either side of conductive bridges 10 and 10a, e.g. between the bridges 10 and 10a; between bridge 10 and spacing link portion 4a, etc.

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Figure 6 illustrates a schematic electrical of the device shown in Figure 5 but tuned only with the above mentioned bridges 10 and 10a. The reference numeral 12 designates the base or main initial impedance (i.e. resistance) represented by region 2 as a whole. The reference numerals 14 and 16 represent respective secondary defined by bridges 10 and 10a.

Although figure 5 shows bridges which are of more or less similar length dimensions, bridges spanning the gap regions 5 for structures such as shown in figures 3 and 4



may not only have different lengths but also different resistances based on such different lengths.

Turning to Figure 7, arrow 18 depicts the direction of application of a focused heating source pulse onto the semiconductor device 1. As may be understood, a focussed heating source may be disposed (not shown) above the integrated semiconductor device 1, and which may apply a pulse 18 to the device 1. As may be understood, the dimensions of the pulse 18 and of the device 1 may not be to scale.

Figure 7, also shows, in enlarged fashion, a cross sectional view of the tunable integrated semiconductor device 1 through the solidified bridge 10 as shown in Figure 5. The solidified bridge 10 was obtained by the application of a focused heating pulse 18 to a pre-selected or pre-determined area comprising a portion of lightly doped gap region 5, as well as adjacent portions 19 and 21 of heavily doped link portions 3 and 4 respectively (shown in dotted lines), so as to melt the affected areas and obtain a melted pool (eventually solidifying into bridge 10. As may be appreciated, a portion of heavily doped link portions 3 and 4 is included in the melted pool. The extent of heavily doped regions 3 and 4 which will melt subsequent to the application of the heating pulse 18 may depend on the characteristics of the heating pulse, namely the power of the pulse, the duration of the application of the pulse, the diameter of the pulse, etc...; the diameter of the heating pulse may for example be such as to span a portion of the gap region and encompass a portion of both of heavily doped link portions 3 and 4. The longer melted pool is melted, the greater the diffusion of dopant from heavily doped regions 3 and 4 into lightly doped region 5. However, the amount of dopants which will diffuse from heavily doped portions 3 and 4 into lightly doped gap region 5 may also depend on how much of heavily doped regions 3 and 4 may be caught by the focussed heating beam 18, i.e. if a large part of heavily doped regions 3 and/or 4 are caused to be melted, more dopants may diffuse, and if a small part is caused to be melted, fewer dopants may diffuse. Depending on the length of time that the melted pool remains melted, the dopant profile across the melted pool from heavily doped region 3 to heavily doped region 4 may not be uniform. Although it is advantageous to form a conductive

bridge between link portions 3 and 4 by use of a single heating pulse spanning the gap region 5, it may if so desired be possible to use a plurality of smaller diameter heating pulses. If a plurality of heating pulses are applied they may be applied in stepwise fashion starting for example from an initial step comprising melting a portion of one link portion and an adjacent portion of the gap region 5 and then proceeding in stepwise fashion across the gap region 5 to finally melt a portion of the other link portion and an adjacent portion of the gap region 5.

Turning to Figures 8 and 9 there is illustrated a representation of a general embodiment of an apparatus 100 for modifying the impedance of an integrated semiconductor device using a focused heating source, such as a laser. An integrated circuit 110 is placed on a positioning table 10, and may be subjected to an application of a heating source 105 which is produced by a focused heating source 103. Heating source 105 may be focused on integrated circuit 110 by using optic or magnetic lenses 107, and a system of cameras and mirrors allows for the observation of the integrated circuit 110 in order to ensure accurate alignment of the heating source 105. Figure 12 shows apparatus 100 in greater detail. Laser 103 is connected to shutter 116, each of which is controlled by the control system shown as a computer 108. Also connected to computer 108 is the control mechanism 109 of the positioners 101. The apparatus 100 further comprises a camera 112, and a light source 114. A further component of the apparatus 100 is a beam splitter 113, and a selective mirror 120.

Turning to Figures 10 to 13, these figures illustrate examples of possible applications of the present invention.

FIG. 10 illustrates an example electric schematic of an example series resistor ladder for an analogue to digital converter which provided with a number of resistance members each generally designated as R. FIG. 11 illustrates how the series resistor ladder of Fig 10 may be formed using a plurality of integrated semiconductor devices as shown in Figure 5; i.e. each device of Fig. 5 may be disposed so as to each define a respective

resistance or impedance member of the analogue to digital converter of example 10; one of the devices, as shown in Figure 5, and which defines a resistance R is shown as being designated by the reference numeral 130 in Figure 11. Once the general structure of Fig 11 is formed by conventional techniques (i.e. laying down of appropriately doped layers, substrates and regions, etc.) fine tuning of each of the members 130 may be carried out as described herein.

FIG. 12 illustrates an example electric schematic of an R-2R resistor ladder for a digital to analogue converter provided with a number of resistance members each generally designated either as R or 2R; FIG. 13 illustrates how a plurality of integrated semiconductor devices as shown in Figure 5 may be disposed so as to define the analogue to digital converter of example 12. Reference numerals 140 and 150 generally designate devices of figure 5 which define respectively a resistance R or 2R. Once the general structure of Fig 13 is formed by conventional techniques (i.e. laying down of appropriately doped layers, substrates and regions, etc.) fine tuning of each of the members 140 and 150 may be carried out as described herein.

FIG. 14 illustrates an example of another tunable integrated semiconductor device of the present invention wherein one of the link portions of the crimp or fold element is not (initially) in the main conductive path. The device 154 comprises various layers or regions, for example, a non-conductive substrate 156, and a conductive layer or region 158 which is contiguous with the underlying substrate 156. In this case, the conductive layer or region 158 comprises a gross, major or large link portion 160 and a minor link portion 161. The large link portion 160 corresponds to the first conductive link portion which defines the base conductive path of the device; thus the major or large link portion 160, itself alone initially forms the main conductive path between contact members 162 and 164, i.e. current is at least initially able to pass through the entire region 158 between these contact members 162 and 164. The minor link portion 161 which is electrically connected at one end thereof to the major link portion by connector member 168, is spaced apart from the link portion 160 by a gap region 170 which is part of the substrate 156. The impedance (i.e. resistanc ) of the device of Fig. 14 is

modified (i.e. lowered) by providing conductive bridges across the gap region 170 as described above with respect to the device of Fig. 5. The creation of the conductive bridges across the gap region 170 will modify the effective (electrical) dimension of the device so as to slightly change the overall resistance of the device 154. This gap/link configuration may be used to provide a more precise tuning of the resistance of a device than by the devices shown in Fig.1 to 5.

FIG. 15 illustrates an example combination of an integrated semiconductor device as shown in Figure 5 with an integrated semiconductor device as shown in Figure 14 to provide a device which may be tuned with higher precision than would be obtainable by the device of FIG. 5 alone. For this overall device initial tuning of the structure of Fig. 5 may give a precision of for example 0.01% whereas tuning of the structure of Fig. 14 may give an overall precision for the device of 0.001%.

The device of Figure 15 also has contact or connector members 8 and 174 for electrically connecting the conduction region(s) to other devices, current is at least initially able to pass through the entire region(s) a between these contact members.

**WE CLAIM:**

1. A method for modifying the impedance of a semiconductor component, said semiconductor component comprising

5 a first conductive region comprising a conductive crimp element, said first region having a heat modifiable dopant profile, said conductive crimp element defining an base conductive path,

and

10 a second region contiguous with the first region, said second region having a dopant profile rendering said second region non-conductive relative to said first region,

said crimp element comprising a first link portion and a second link portion,

15 said first and second link portions being disposed in juxtaposition such that said first and second link portions are separated by a gap region defined by said second region, said second region having a heat modifiable dopant profile, at least with respect to said gap region,

20 said method comprising applying a bridging cycle to at least one preselected area, each said preselected area comprising at least a portion of each of said first link portion, said second link portion and said gap region, so as to form a discrete conductive bridge across said gap region and connecting said first link portion and said second link portion,

said bridging cycle comprising a heating/cooling treatment comprising

25 directing a focussed heating source to melt said preselected area and to thereby alter the dopant profile of the pre-selected area

and

allowing said melted pre-selected area to solidify with an altered dopant profile so as to form thereby said discrete conductive bridge.

- 30 2. A method as defined in claim 1 further including the steps of

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a) determining the impedance of said semiconductor component subsequent to a bridging cycle and

b) comparing the impedance obtained from step a) with a predetermined impedance

5 and

c) if necessary, repeating, at one or more additional pre-selected areas, said bridging cycle, until said predetermined impedance is achieved, each bridging cycle being applied to a different pre-selected area to form a respective discrete conductive bridge.

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3. A method for modifying the impedance of a semiconductor component, said semiconductor component comprising

15 a first conductive region defining a base conductive path, said first conductive region comprising a first link portion and a second link portion, said first region having a heat modifiable dopant profile

and

20 a second region contiguous with the first region, said second region having a dopant profile rendering said second region non-conductive relative to said first region,

25 said first and second link portions being disposed in juxtaposition such that said first and second link portions are separated by a gap region defined by said second region, said second region having a heat modifiable dopant profile, at least with respect to said gap region,

30 said method comprising applying a bridging cycle to at least one preselected area, each said preselected area comprising at least a portion of each of said first link portion, said second link portion and said gap region, so as to form a discrete conductive bridge across said gap region and connecting said first link portion and said second link portion,

said bridging cycle comprising a heating/cooling treatment comprising  
directing a focussed heating source to melt said preselected area and to  
thereby alter the dopant profile of the pre-selected area  
and  
5 allowing said melted pre-selected area to solidify with an altered dopant  
profile so as to form thereby said discrete conductive bridge.

4. A method as defined in claim 3 further including the steps of

- 10 a) determining the impedance of said semiconductor component  
subsequent to a bridging cycle and  
b) comparing the impedance obtained from step a) with a predetermined  
impedance

and

- 15 c) if necessary, repeating, at one or more additional pre-selected areas,  
said bridging cycle, until said predetermined impedance is achieved, each  
bridging cycle being applied to a different pre-selected area to form a  
respective discrete conductive bridge.

20  
5. A method for modifying the impedance of a semiconductor component, said  
semiconductor component comprising

25 a first conductive region comprising a first conductive link portion and a  
second link portion, said first region having a heat modifiable dopant  
profile, said first conductive link portion defining a base conductive path

and

30 a second region contiguous with the first region, said second region  
having a dopant profile rendering said second region non-conductive  
relative to said first region,

said first and second link portions being disposed in juxtaposition such that said first and second link portions are separated by a gap region defined by said second region, said second region having a heat modifiable dopant profile, at least with respect to said gap region,

5           said method comprising applying a bridging cycle to at least one preselected area, each said preselected area comprising at least a portion of each of said first link portion, said second link portion and said gap region, so as to form a discrete conductive bridge across said gap region and connecting said first link portion and said second link portion,

10           said bridging cycle comprising a heating/cooling treatment comprising  
              directing a focussed heating source to melt said preselected area and to thereby alter the dopant profile of the pre-selected area

              and

15           allowing said melted pre-selected area to solidify with an altered dopant profile so as to form thereby said discrete conductive bridge.

6.       A method as defined in claim 5 further including the steps of

20           a) determining the impedance of said semiconductor component subsequent to a bridging cycle and

              b) comparing the impedance obtained from step a) with a predetermined impedance

and

25           c) if necessary, repeating, at one or more additional pre-selected areas, said bridging cycle, until said predetermined impedance is achieved, each bridging cycle being applied to a different pre-selected area to form a respective discrete conductive bridge.



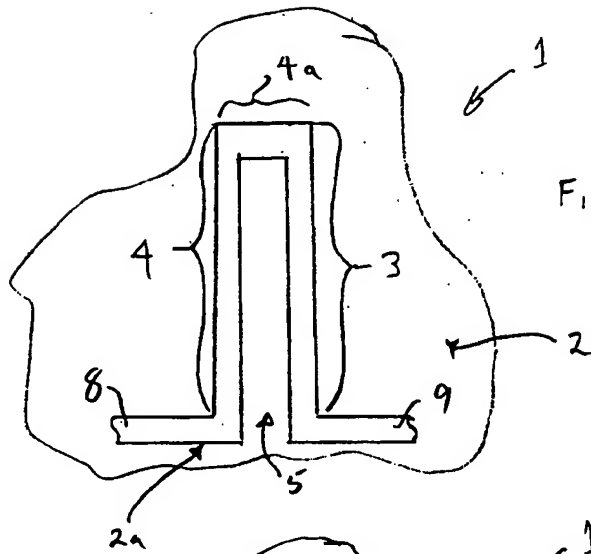


Figure 1

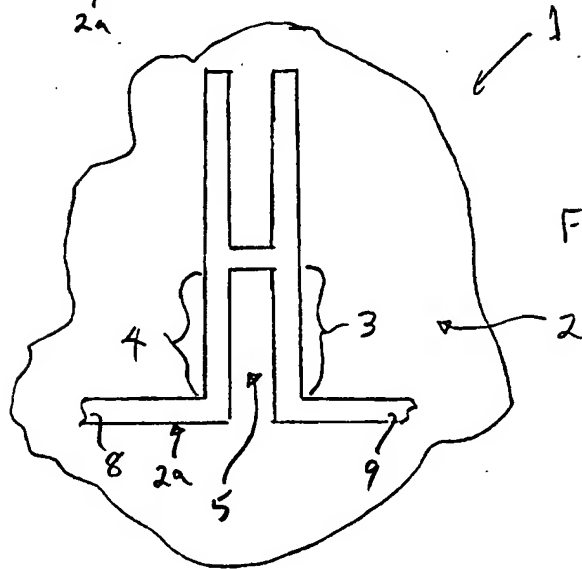
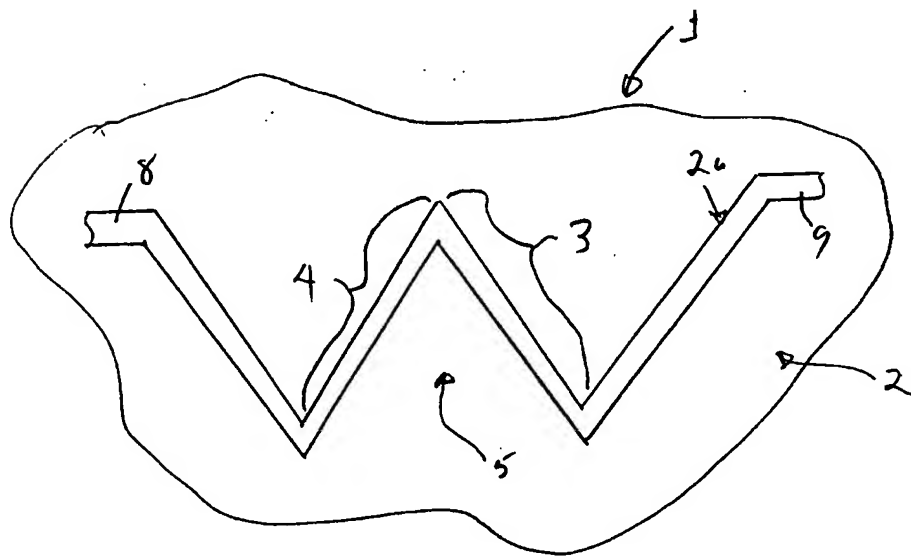
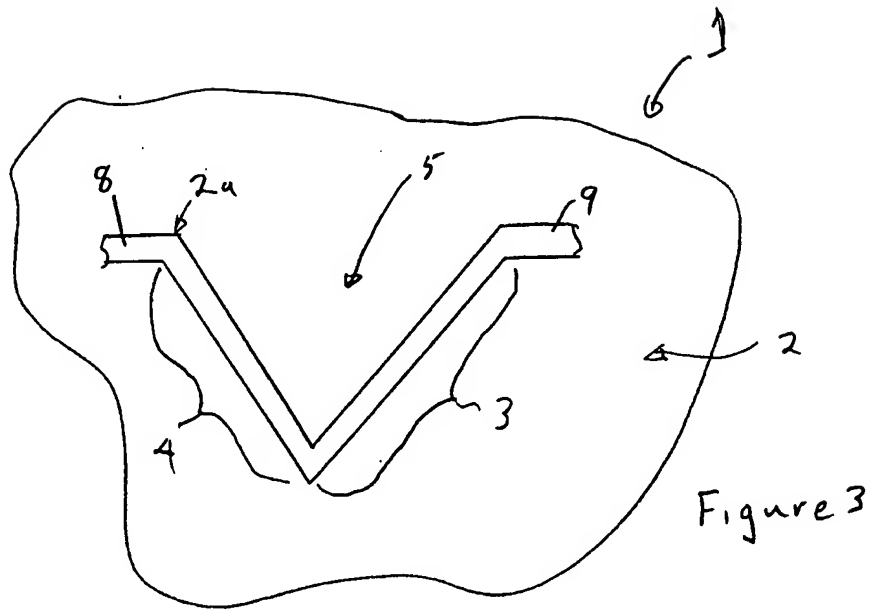


Figure 2



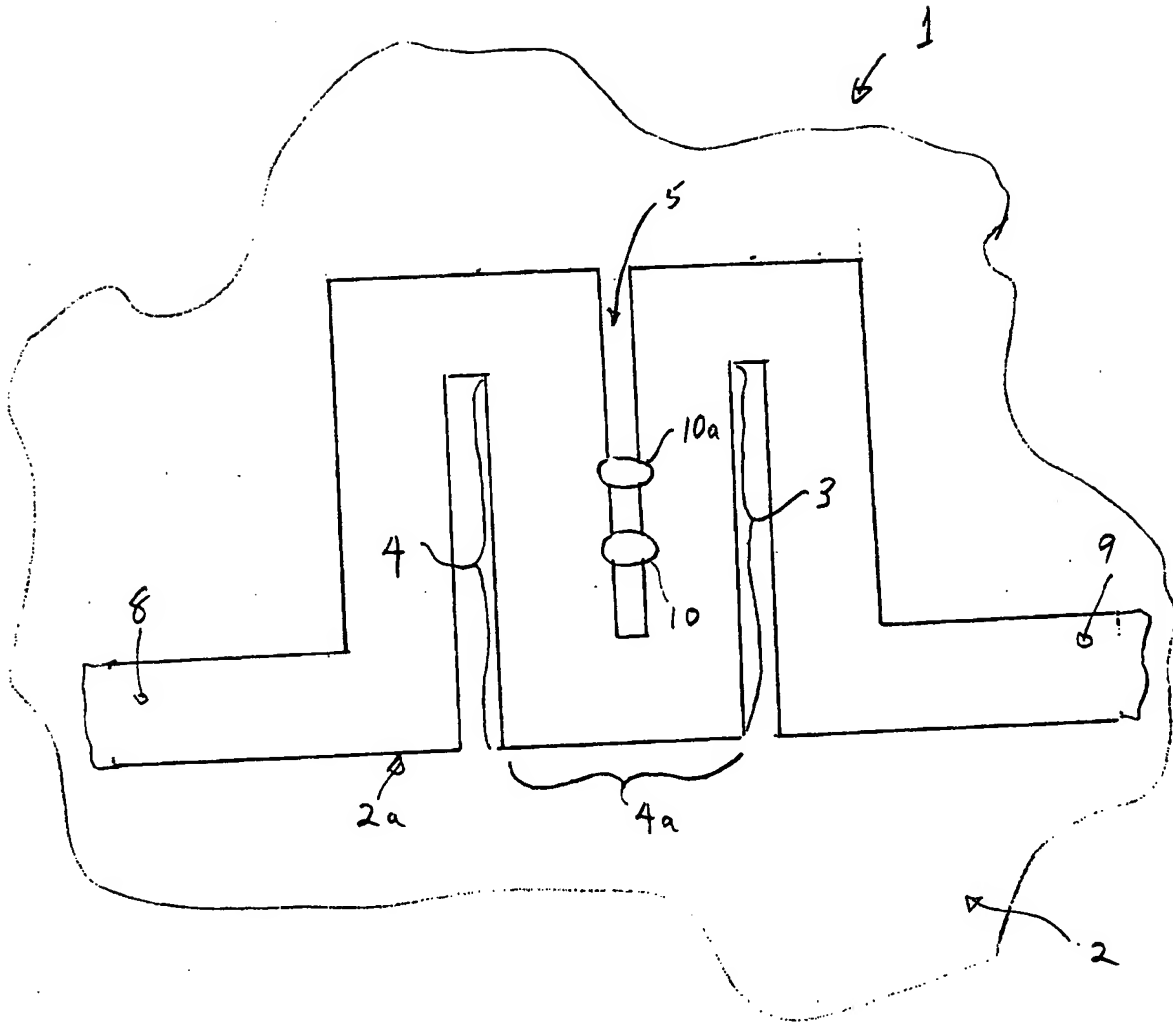


Figure 5

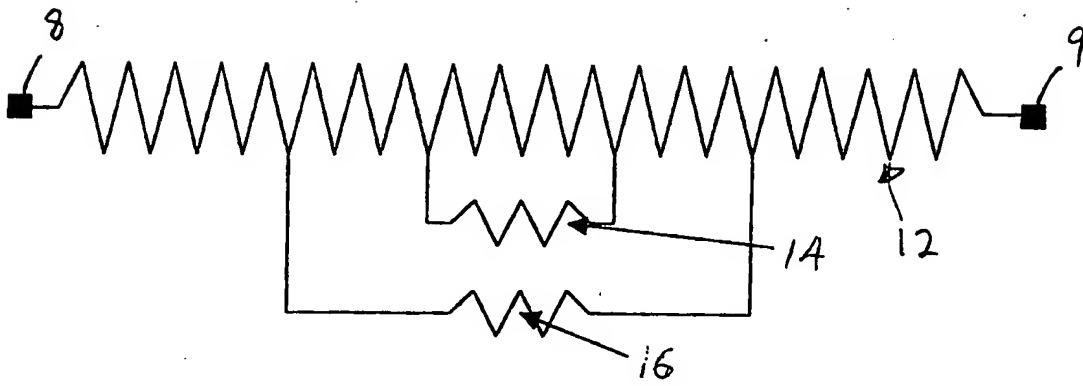
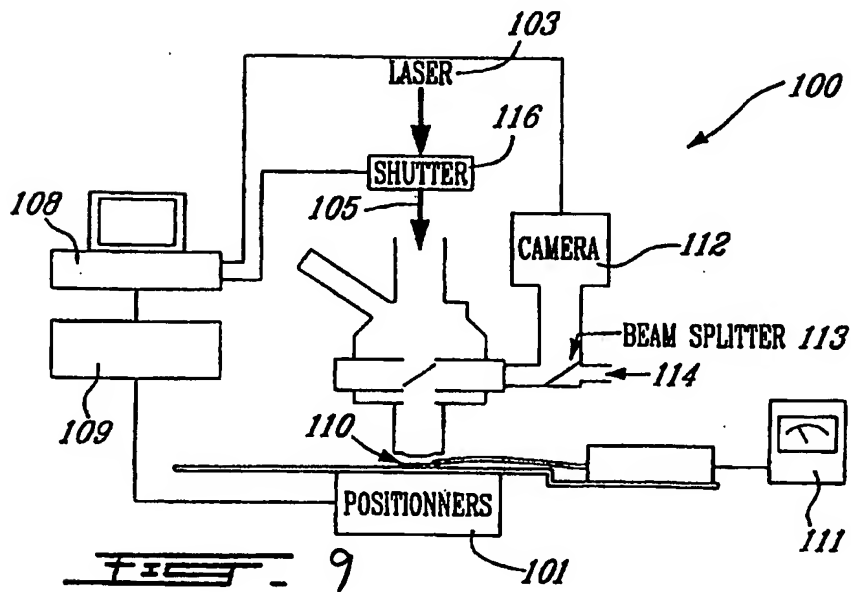
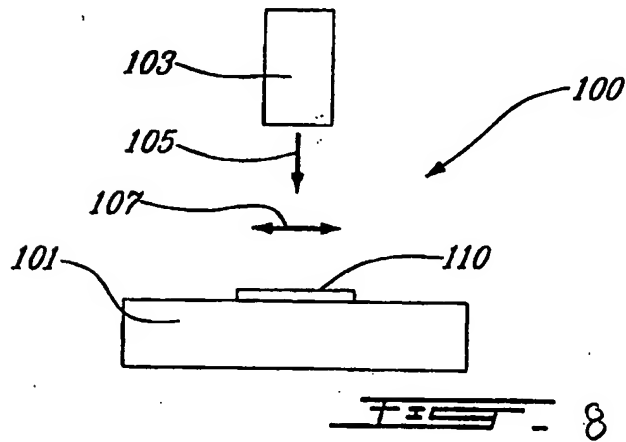
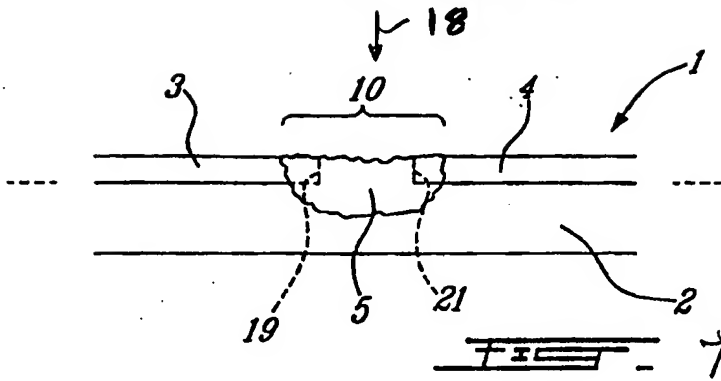


Figure 6



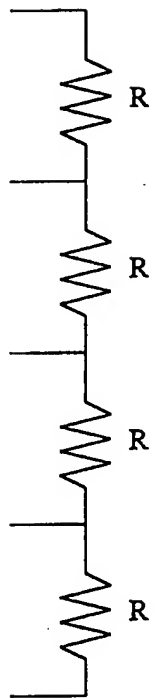


Figure 10

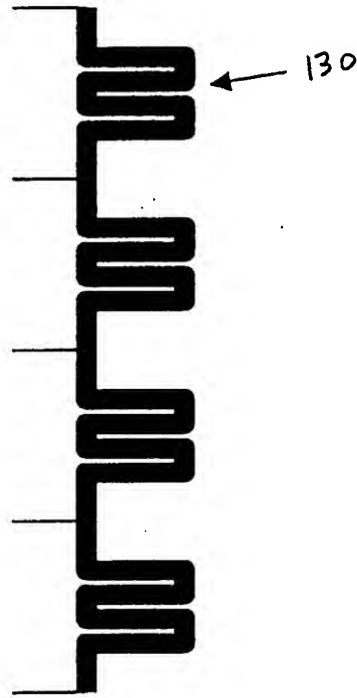


Figure 11

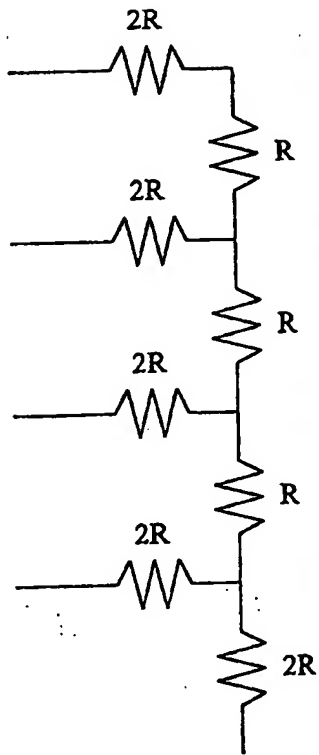


Figure 12

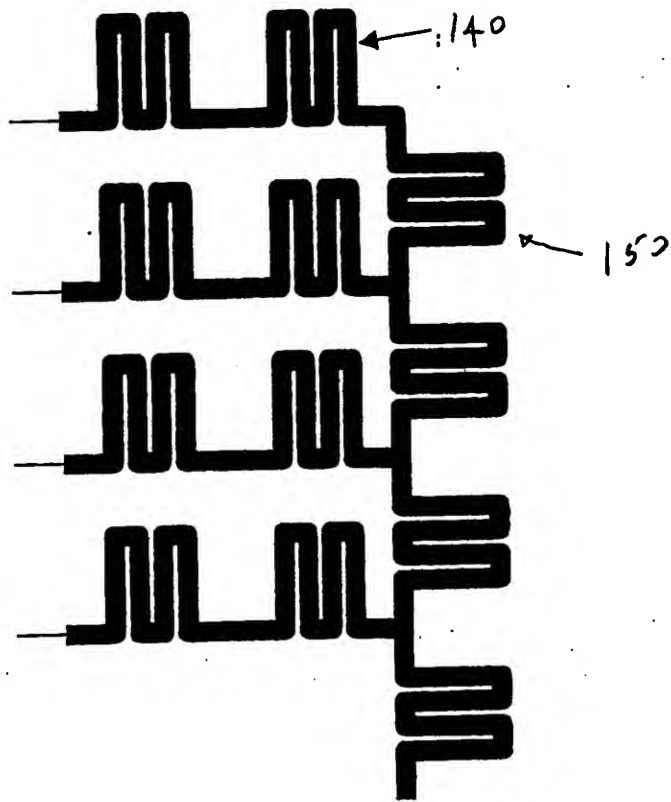


Figure 13

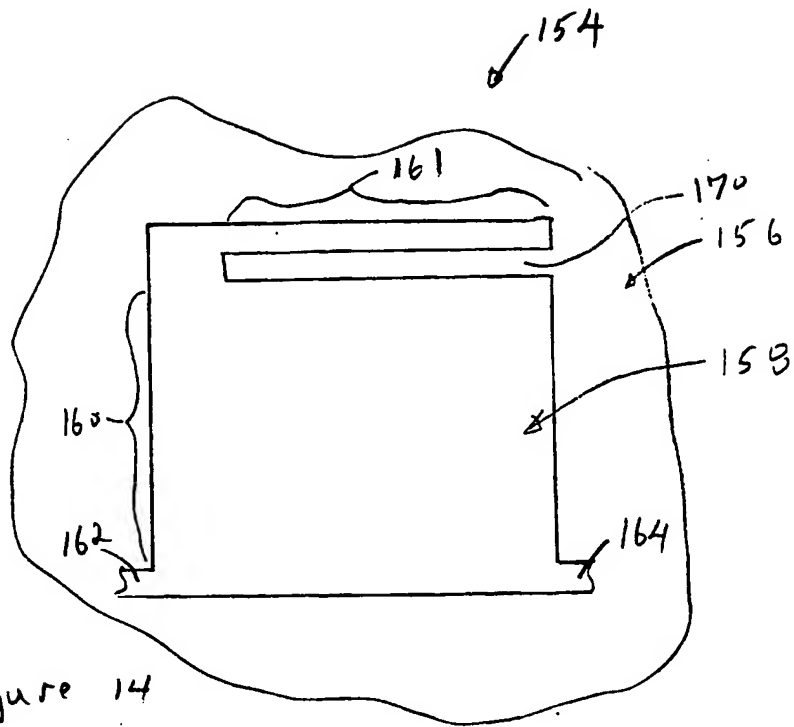


Figure 14

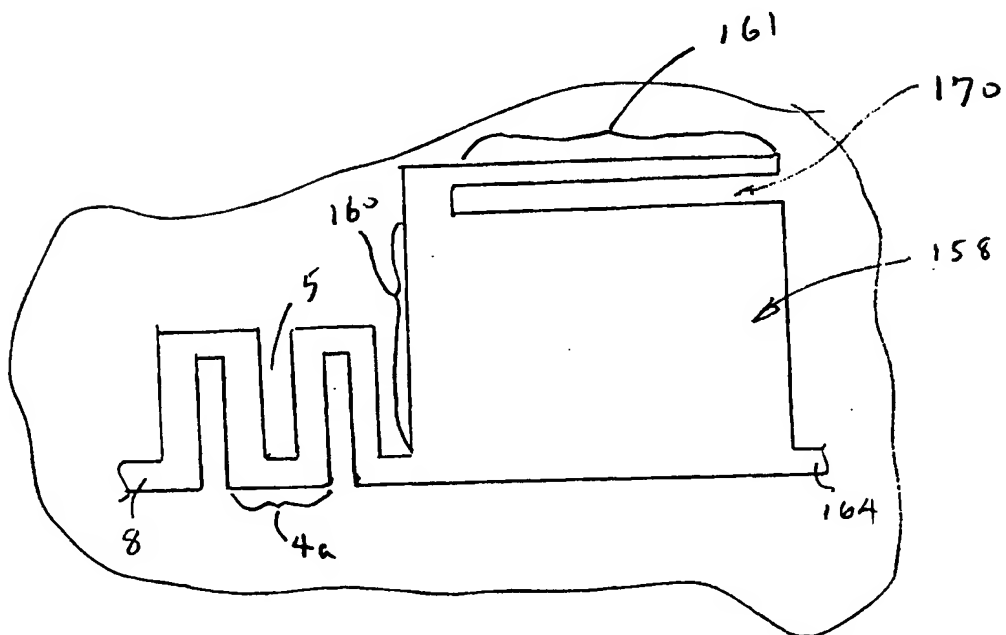


Figure 15